

Design of a Low-Cost, Underwater Acoustic Modem for Short-Range Sensor Networks

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Abstract- A fundamental impediment to the use of dense underwater sensor networks is an inexpensive acoustic modem. Commercial underwater modems that do exist were designed for sparse, long range, applications rather than for small, dense, sensor nets. Thus, we are building an underwater acoustic modem starting with the most critical component from a cost perspective – the transducer. The design substitutes a commercial transducer with a homemade transducer using cheap piezo-ceramic material and builds the rest of the modem’s components around the properties of the transducer to extract as much performance as possible. This paper presents the design considerations, implementation details, and initial experimental results of our modem.

I. INTRODUCTION

Our fundamental knowledge of aquatic ecosystems is increasing at a tremendous rate due to the physical, chemical and biological time-series data from long term sensors. As a result, research sites around the world are being equipped with a broad range of sensors and instruments. Despite the substantial effort to monitor ecological aspects of aquatic systems, the infrastructure needed for sensor networks in marine and freshwater systems without question lags far behind that available for terrestrial counterparts.

There is increasing interest in the design and deployment of underwater acoustic communication networks. For example, the Persistent Littoral Undersea Surveillance Network (PLUSNet) demonstrates multi-sensor and multi-vehicle anti-submarine warfare (ASW) by means of an underwater acoustic communications network [1]. A short range shallow water network to monitor pollution indicators in Newport Bay, CA is proposed in [2]. A network of acoustic modems akin to motes is proposed for low power, short range acoustic communications for seismic monitoring [3]. A swarm of acoustically networked autonomous drifters is envisioned to monitor phenomena as they are subjected to ocean currents [4]. A 1km x 1km underwater wireless network of 10s of temperature sensors is envisioned to obtain high temporal and spatial resolution observations within the coral reef lagoon at the Moorea Coral Reef Long Term Ecological Research Station [5].

In order to make more short-range underwater acoustic communication networks a reality, the cost of underwater acoustic modems must come down. Commercial off-the-shelf (COTS) underwater acoustic modems are not suitable for short-range (~ 100m) underwater sensor-nets: their power draws, ranges, and price points are all designed for sparse,

long-range, expensive systems rather than small, dense, and cheap sensor-nets [6]. It is widely recognized that an open-architecture, low cost underwater acoustic modem is needed to truly enable advanced underwater ecological analyses.

Underwater acoustic modems consist of three main components (Figure 1): (1) an underwater transducer, (2) an analog transceiver (matching pre-amp and amplifier), and (3) a digital platform for control and signal processing. A substantial portion of the cost of the modem is the underwater transducer; commercially available underwater omnidirectional transducers (such as those as seen in existing research modem designs [7-9]) cost on the order of \$2K-\$3K. Commercial transducers are expensive, due to the cost of ensuring consistent quality control of manufacturing piezoelectric materials and potting compounds, expensive calibration equipment and time-consuming characterization, all further exacerbated by low volume production. Therefore, much of the design for the low-cost modem lies in finding an appropriate substitute for the custom commercial transducer. Jurdak et al. substituted the transducer with generic, inexpensive, speakers and microphones, but were only able to obtain a data rate of 42 bps for a transmission range of 17m [10]. Benson et. al substituted a custom transducer with a commercially available fish finder transducer (which cost \$50), but was only able to obtain a data rate of 80 bps for a transmission range of 6m [11]. Furthermore, these fish finders have a < 5 degree beam width, making them less than ideal for most deployment scenarios.

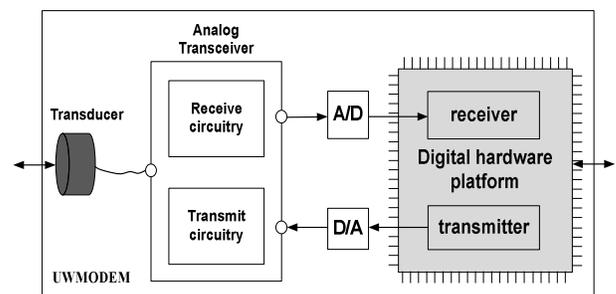


Figure 1. Major components of an underwater acoustic modem

In this paper, we present the design of a short-range underwater acoustic modem starting with the most critical component from a cost perspective – the transducer. The design substitutes a commercial underwater transducer with a homemade underwater transducer using cheap piezoceramic

material and builds the rest of the modem's components around the properties of the transducer to extract as much performance as possible. We describe the design considerations, implementation details, and initial experimental results of our modem prototype.

The remainder of this paper is organized as follows. Section II describes the design of our homemade transducer and its experimentally determined electrical and mechanical properties. Section III describes the design of our analog transceiver and Section IV describes the design transceiver. We present experimental results in Section V and compare the power and cost of our modem to existing modem designs in Section VI. We conclude with a discussion on future work in Section VII.

II. TRANSDUCER

In this section we describe the design of our homemade transducer, explaining the reasons behind the selection of its piezo-ceramic, urethane compound, and wire leads. We then present the transducer's experimentally determined electrical and mechanical properties which are used to govern the rest of the modem design.

A. Transducer Design

Underwater transducers are typically made from piezoelectric materials – materials (notably crystals such as lead zirconate titanate and certain ceramics) that generate an electric potential in response to applied mechanic stress and produce a stress or strain when an electric field is applied. For underwater communication, transducers are usually omnidirectional in the horizontal plane to reduce reflection off the surface and bottom. This is especially important for shallow water communications.

The 2D omni-directional beam pattern can be achieved using a radially expanding ring or using a ring made of several ceramics cemented together. A radially expanding ceramic ring provides 2D omni-directionality in the plane perpendicular to the axis and near omni-directionality in planes through the axis if the height of the ring is small compared to the wavelength of sound being sent through the medium [12]. The radially expanding ceramic is relatively inexpensive to manufacture. A ring made of several ceramics cemented together provides greater electromechanical coupling, power output, and electrical efficiency; the piezoelectric constant and coupling coefficient are approximately double that of a one-piece ceramic ring [Ken1]. They work better because the polarization can be placed in the direction of primary stresses and strains along the circumference. However, these are much more difficult to manufacture and are therefore much more expensive than a one piece radial expanding piezoelectric ceramic ring. We thus selected to use a single radially expanding ring, a <\$10 Steminc model SMC26D22H13SMQA to achieve an omni-directional beam pattern at low-cost.

The most common method of making transducers from a ring ceramic is to add two leads, and pot it for waterproofing [12]. We used shielded cables for the transducer leads to

ensure the leads would not pick up unwanted electromagnetic noise and attached the leads using solder with 3% silver.

The piezoelectric ceramic needs to be encapsulated in a potting compound to prevent contact with any conductive fluids. Urethanes are the most common material used for potting because of their versatility. The most important design consideration is to find a urethane that is acoustically transparent in the medium that the transducer will be used; this is more important for higher frequency or more sensitive applications where the wavelength and amplitude is smaller than the thickness of the potting material. Generally, similar density provides similar acoustical properties. Mineral oil is another good way to pot the ceramics because it is inert and has similar acoustical properties as water. Some prefer using mineral oil to urethane because it is not permanent. However, the oil still needs to be contained by something, which is often a urethane tube. We selected a two-part urethane potting compound, EN12, manufactured by Cytec Industries [13] as it has a density identical to that of water, providing for efficient mechanical to acoustical energy coupling.

Creating a transducer by potting the ceramic shifts its resonance frequency due to the additional mass moving immediately around the transducer. The extent of the shift depends on the potting compound's characteristics. Characteristics can vary depending on the type, age, temperature, and mixing method of the compound. The amount of potting can influence resonance frequency as well. Having tight control over these variables to ensure exact reproducibility requires expensive equipment. To keep costs low, we used a simplistic potting method, pouring and mixing the compound by hand in a thermostat controlled lab. Experimental results described in the next subsection indicate that the transducer variations caused in our simplistic potting procedure are suitable for our intended application.

Figure 2 shows the piezo-ceramic ring, the potted ceramic, and the transducer in the potting compound mounted to a prototype plate to be attached to the modem housing. The total cost of our transducer, including the ceramic, leads, potting and labor is approximately \$50.

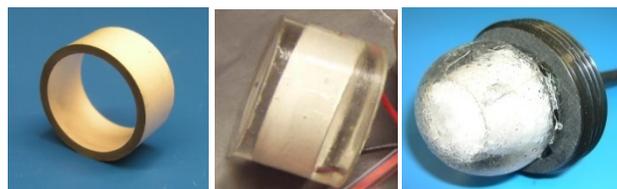


Figure 2. From left to right: The raw piezoelectric ring ceramic, the potted ceramic, the transducer in the potting compound mounted to a prototype plate to be attached to a modem housing.

B. Transducer Properties

For a single radially expanding ceramic ring, the resonance frequency occurs when the circumference approximately equals the operating wavelength [12, 14]. In air, this frequency is about 41 kHz for every inch in diameter of a solid radially expanding ceramic ring; for the ring made of several ceramics cemented together, in the case that there is not inactive material (such as electrodes or cement), the resonance

frequency is approx 37 kHz for every inch [12]. The SMC26D22H13SMQA has an outer diameter of 1.024 inches, a wall thickness of 0.1 inches and a height of 0.512 inches.

Steminc specifies that the ceramic ring has a nominal resonance frequency of 43kHz +/- 1.5kHz. Experimentally measuring the impedance of two different ceramics (Figure 3) shows the ceramics do fall within this specification. The resonance frequency (~43kHz) and anti-resonance frequency (~45kHz) occur at minimum and maximum impedances, respectively [14, 15].

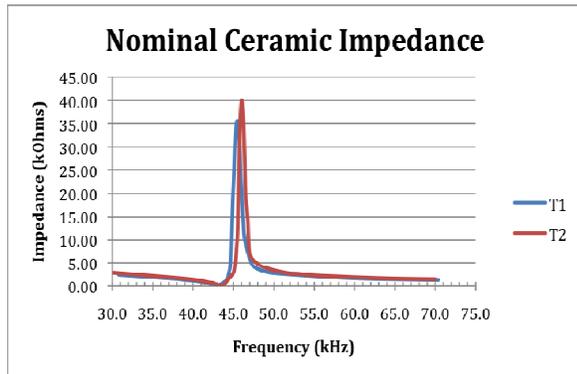


Figure 3. The SMC26D22H13SMQA ceramic impedance (and resonance frequency) in air of two ceramics (T1, T2)

As stated in the previous subsection, potting the ceramic shifts the resonance frequency due to the additional mass moving immediately around the transducer. Figure 4 shows the extent of this shift and the relatively small variation (caused by the ceramic's variation and the potting procedure) between two different transducers (potted using the ceramics T1 and T2 from Figure 3). Transmitting around the transducer's resonance frequency (35kHz) provides the most efficient electrical to acoustical energy coupling [12,14].

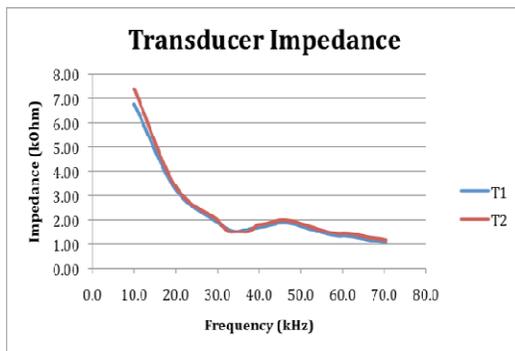


Figure 4. The transducer impedance and resonance frequency (~35kHz) of transducers potted from ceramics T1 and T2

To characterize the transducer's electro-mechanical properties, we experimentally measured its transmitting voltage response (TVR) and its receiving voltage response (RVR). The TVR is defined as the sound pressure level experienced at 1m range, generated by the transducer per 1 V of input Voltage and is a function of frequency. The RVR is a measure of the voltage generated by a plane wave of unit acoustic pressure at the receiver and is a function of frequency.

The experimental procedure to determine the transducer's TVR and RVR included placing our transducer in water 1 meter apart from a reference transducer with a known TVR and RVR (in our case, an ITC1042 [16]) in the middle of a 3 meter deep, 2 meter wide cylindrical test tank, and collecting signals swept across frequencies, 31k-90kHz in 1kHz increments, sent from the reference transducer to our transducer and vice versa. We then calculated the RVR and TVR of our transducer based on the collected data and the reference's TVR and RVR. Figures 5 and 6 show the TVR and RVR of transducer T1.

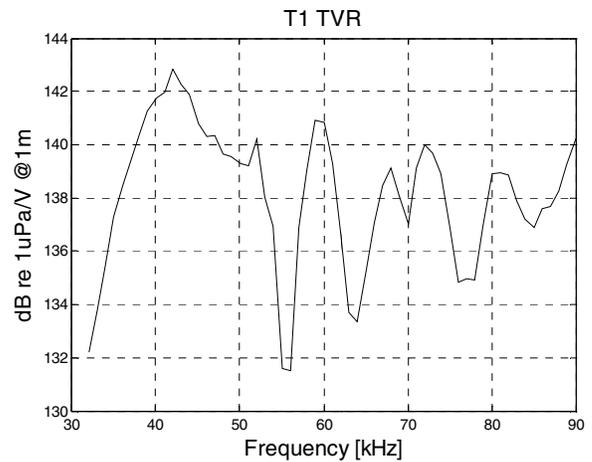


Figure 5. Experimentally determined transmitting voltage response for transducer T1

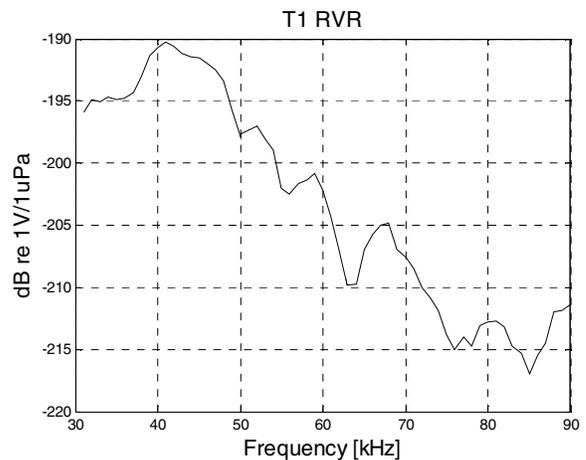


Figure 6. Experimentally determined receiving voltage response for transducer T1

The max response of the TVR and RVR do not necessarily occur at the transducer's electrical resonance (as seen in Figures 5 and 6), but the transducer's resonance frequency still falls near the peak. The sharp peaks and valleys of TVR and RVR can be attributed to inefficiencies in the calibration procedure and characteristics of resonance that are directly related to geometry of the PZT. To obtain a flatter, smoother TVR and RVR (such as those for [16]), more expensive ceramics and manufacturing and calibration procedures are required.

In addition to the TVR and RVR, an important parameter of a transducer is how much voltage it can tolerate before it breaks. A typical Type I PZT's can experience up to 12 volts AC per .001 inches wall thickness without much effect to its electro-mechanical properties[17]. Thus, voltages up to 1200Vpp or 425Vrms should be used for our transducer.

Using the passive sonar equation we can calculate the expected max distance the transducer will be able to send a signal given a Source Level (SL), the transmission loss (TL, due to spreading and absorption loss in the water), and the noise level (NL) of the ocean.

$$SNR = SL - TL - NL \quad (1)$$

Figure 7 shows the expected max distance achievable for the transducer transmitting at the transducer's resonance frequency at various voltages assuming a noise level of 50 dB r 1 uPa.. Transmitting 425 Vrms, for an SNR of 10 dB re 1 uPa at the receiver, the transducer could theoretically send a signal up to 2800 meters. The receive voltage at 10 dB SNR (determined using the RVR) is 820uV.

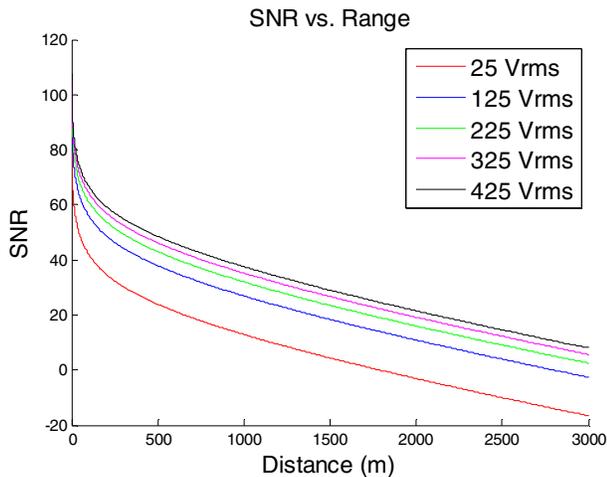


Figure 7. SNR vs. range for various transmit voltages based on transducer T1's TVR. The graph assumes transmission at 35kHz and an ocean noise level of 50 dB re 1uPa.

The transducer's experimentally determined electrical and mechanical properties govern the design choices for the rest of the modem design. The following section describes the analog transceiver.

III. ANALOG TRANSCEIVER

The analog transceiver (Figure 8) consists of a high power transmitter and a highly sensitive receiver both of which are optimized to operate in the transducer's resonance frequency range (Figure 4). The transmitter is responsible for amplifying the modulated signal from the digital hardware platform and sending it to the transducer so that it may be transmitted through the water. The receiver amplifies the signal that is detected by the transducer so that the digital hardware platform can effectively demodulate the signal and analyze the transmitted data. The transceiver costs between \$125 and \$225

per unit depending on the quantity produced. The transmitter and receiver portions of the analog transceiver are described in more detail in the following subsections.



Figure 8. Analog Transceiver

C. Analog Transmitter

The transmitter was designed to operate for signal inputs in a range of 0 – 100kHz. The architecture is unique and consists of two different amplifiers working in tandem (Figure 9). The primary amplifier is a highly linear Class AB amplifier that provides a voltage gain of 23 while achieving a power efficiency of about 50%. The output of the Class AB amplifier is connected to current sense circuitry that in turn controls the secondary amplifier, which is a Class D switching amplifier. The Class D amplifier is inherently nonlinear but possesses an efficiency of approximately 95%. With both of the amplifiers driving the load and working together, the transmitter achieves a highly linear output signal while maintaining a power efficiency greater than 75%. Due to its high linearity, the transmitter may be used with any modulation technique that can be programmed into the digital hardware platform.

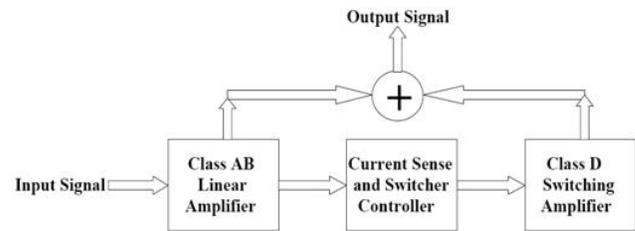


Figure 9. Analog transmitter block diagram. The transmitter uses two amplifiers to achieve efficiency

A power management circuit is provided to adjust the output power in real-time to match it to the actual distance between transmitter and receiver. The ability to provide a low-power output has several important benefits: (1) less interference for nearby ongoing communications; (2) reduced noise pollution and (3) considerable power savings. The current configuration of the transmitter is equipped with a power management system that can switch between output levels of 2, 12, 24 and 40 watts. The power management system has been designed so that the transmitter will maintain maximum efficiency over this wide range of power output

levels. The system is controlled by a low current 5 volt signal from the digital hardware platform so that the power may be dynamically controlled for different operating conditions.

D. Analog Receiver

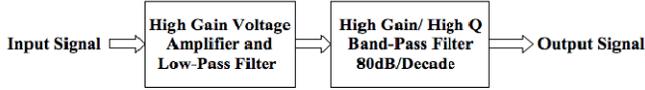


Figure 10. Analog receiver block diagram. The receivers provides high gain in a narrow band around the transducer’s resonance

The receiver’s architecture consists of a set of narrow (high Q) filters with high gain (Figure 10). These filters are based on biquad band-pass filters, and essentially combine the tasks of filtering and amplification. The receiver is configured so that it only amplifies signals around 35 kHz (to match the electrical resonance frequency of the transducer) while attenuating low frequencies at a rate of 120dB per decade and high frequencies at rate of 80dB per decade (Figure 11). The receiver must be able to amplify only the frequencies of interest because of the large amount of noise associated with underwater acoustic signals. The current receiver configuration consumes about 375 mW when in standby mode and less than 750 mW when fully engaged. The relatively high power consumption (in comparison to that of the WHOI Micromodem (200mW)) [7] is a result of the receiver’s high gain (65dB) which is capable of sufficiently amplifying an input signal as small as a few hundred microvolts allowing the receiver to pick up signals at longer distances (such as the 820uV received signal described in section II). An ultra-low power wake up circuit will be added to the receiver to considerably reduce power consumption. A few receiver component values can be changed to widen its bandwidth (but decrease its gain) to allow for transmission of modulation schemes that require more bandwidth.

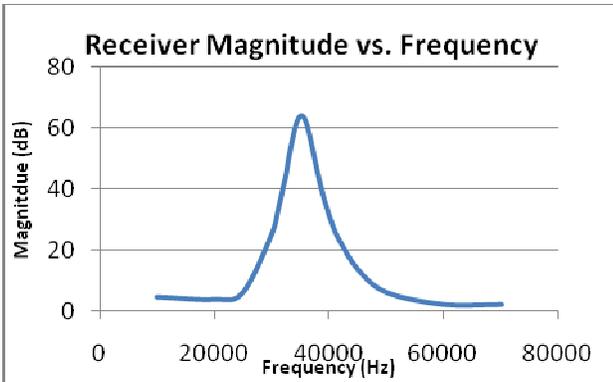


Figure 11. The measured frequency response of the analog receiver

IV. DIGITAL TRANSCEIVER

The digital transceiver is responsible for physical layer communication, i.e., implementing a suitable baseband processing scheme (including modulation, filtering, synchronization, etc.) for the application and environment of interest. There are many design choices that must be considered when designing a digital transceiver for the

underwater acoustic modem including, but not limited to, the choice of modulation scheme and hardware platform for its implementation. We selected to implement frequency shift keying, (FSK) on a field programmable gate array (FPGA) for our modem prototype.

FSK is a fairly simple modulation scheme that has been widely used in underwater communications over the past two decades due to its resistance to time and frequency spreading of the underwater acoustic channel [7,18]. Other modulation schemes such as phase shift keying [7], direct sequence spread spectrum (DSSS) [8] and orthogonal division frequency multiplexing (OFDM) [19, 20] are now being considered for higher data rate underwater applications, but the proven robustness of FSK and its simplicity makes it an attractive modulation scheme as the first prototype for our low-cost, low-power, low-data rate application.

Reconfigurable systems (e.g., FPGAs) are a class of computing architectures that allow tradeoffs between flexibility and performance [21-23]. They strike a balance between solely hardware and solely software solutions, as they have the programmability and non-recurring engineering costs of software with performance capacity and energy efficiency approaching that of a custom hardware implementation [23]. Reconfigurable systems are known to provide the performance needed to process complex digital signal processing applications and especially provide increased performance benefits for highly parallel algorithms [24]. Furthermore, they are programmable allowing the same device to be used to implement a variety of different communication protocols. Once the designs are ready in FPGA, they can relatively easily be moved to an ASIC to reduce both the area, cost and power consumption.

The following subsections describe an overview of the FSK modem implementation and its HW/SW co-design for accurate control and I/O.

A. FSK Modem Design

Table I shows the FSK modem’s time and frequency parameters which were selected based on the properties of the transducer. The ‘mark’ frequency represents the frequency used to represent a digital ‘1’ when converted to baseband and the ‘space’ frequency represents the frequency used to represent a digital ‘0’ when converted to baseband. The sampling frequency is used for sending and receiving the modulated waveform on the carrier frequency while the baseband frequency is used for all baseband processing.

TABLE I.
FSK MODEM PARAMETERS

Properties	Assignment
Modulation	FSK
Carrier frequency	35 KHz
Mark frequency	1 KHz
Space frequency	2 KHz
Symbol duration	5 ms
Sampling Frequency	800 KHz
Baseband Frequency	16 KHz

Figure 12 illustrates a block diagram of our FPGA implementation of an FSK modem. In receive mode, the input

signal adc_in is the received analog signal from the analog to digital converter, sampled at the sampling frequency, which consists of a modulated wave form (when data is present) and noise. The following digital down converter (DDC) recovers the signal to the digital baseband according to the FSK modulation scheme and known carrier frequency and allows for subsequent processing at the lower, baseband frequency. A symbol synchronizer is then required to locate the start of the first symbol of a data packet to set accurate sampling and decision timing for subsequent demodulation. The synchronizer is based on correlation with a known reference sequence (a 15-bit Gold code translated to an FSK waveform where a ‘-1’ is represented with the space frequency and a ‘1’ is represented with the mark frequency). When the reference and receiving sequence exactly align with each other, the correlation result reaches a maximum value and the synchronization point is located. Details of the symbol synchronizer’s implementation can be found in [25]. The demodulator block is disabled until it obtains a valid symbol synchronization clock from the symbol synchronizer. The demodulator adopts a matched filter FSK demodulation scheme described making use of two bandpass filters (one centered on the mark frequency and one centered on the space frequency) to decode the sequence. The decoded bit stream $data_out$ is then sent to the host computer and translated to a readable message.

In transmit mode, the modem receives a bit stream ($data_in$) and modulates the bit stream into an FSK waveform using a cosine look up table. The modulated waveform, sampled at the sampling frequency, is sent to the analog transceiver through the digital to analog converter (dac_out).

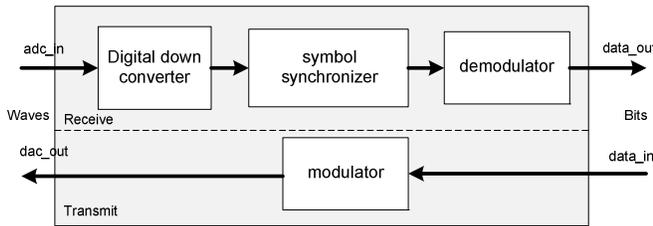


Figure 12. Block diagram of an FPGA implementation of an FSK modem

TABLE II.
FSK MODEM RESOURCES

	Occupied slices	LUTs	BRAMs
Modulator	95	184	9
DDC	284	541	9
Demodulator	1025	1980	1
Synchronizer	12000	22101	2
Total modem	16,706	29,076	55

Each component of the digital modem (modulator, digital down converter, synchronizer, and demodulator) was designed in Verilog and tested individually in ModelSim to verify its operation. Table II shows the FPGA hardware resources occupied for each component of the acoustic modem design

with standard optimization. The resources reported for the total modem include the resources for the complete HW/SW co-design as described in the next subsection (Figure 13). Using the resource values in the XPower Estimator 9.1.03, for an even lower power device, the Spartan-6 XC6SLX150T, the power consumption estimation for the complete modem design is 233 mW.

B. FSK HW/SW Co-design

We used Xilinx Platform Studio 10.1 to design a HW/SW co-design for the digital modem to allow for accurate control and I/O. The co-design consists of the digital modem, a UART (Universal Asynchronous Receiver Transmitter) to connect to serial sensors or to a computer serial port for debugging, an interrupt controller to process interrupts received by the UART or the modem, logic to configure the on board ADC, DAC, and clock generator, and MicroBlaze, an embedded microprocessor to control the system (Figure 13).

The MicroBlaze processor is a 32-bit Harvard reduced instruction set computer (RISC) architecture optimized for implementation in Xilinx FPGAs. It interfaces to the digital modem through two fast simplex links (FSLs), point-to-point, uni-directional asynchronous FIFOs that can perform fast communication between any two design elements on the FPGA that implement the FSL interface. The MicroBlaze interfaces to the interrupt controller and UART core over a peripheral local bus (PLB), based on the IBM standard 64-bit PLB architecture specification.

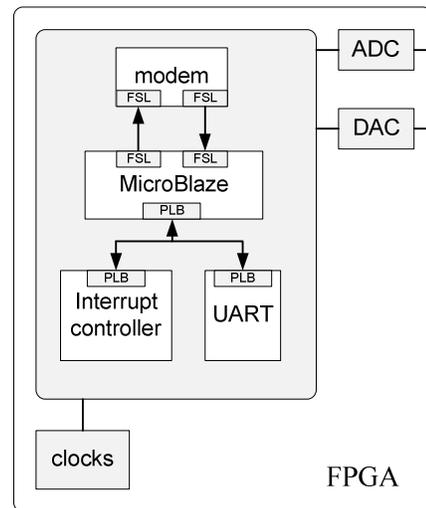


Figure 13. HW/SW Co-Design for the digital modem

Upon start-up, the MicroBlaze initializes communication with the modem by sending a command signal through the FSL bus signaling the modem to turn on. When the modem is ready to begin receiving signals, it sends an interrupt back to MicroBlaze to indicate initialization is complete. The modem then begins the down conversion and synchronization process, processing the signal received from the ADC and looking for a peak above the threshold to indicate a packet has been received. If the modem finds a peak above the threshold, it

finds the synchronization point, and demodulates the packet. The demodulated bits are stored in the FSL FIFO. When the full packet has been demodulated, the modem sends an interrupt indicating a packet has been received and the MicroBlaze may retrieve the packet from the FSL. The modem then returns to synchronization, searching for the next incoming packet.

After initialization, the MicroBlaze remains idle, waiting for interrupts either from the modem or UART. If it receives an interrupt from the modem indicating that a packet has been demodulated, the MicroBlaze reads the bits from the FSL FIFO and sends the bits over the UART to be printed on a computer's Hyperterminal for verification. If the MicroBlaze receives an interrupt from the UART, indicating that the user would like to send data, the MicroBlaze sends a command to the modem to send the bitstream the MicroBlaze places in the FSL. The modem then modulates the data from the FSL and sends the modulated waveform to the DAC for transmission. The MicroBlaze then returns to waiting for interrupts from the modem or the UART and the modem returns to synchronization, searching for the next incoming packet. This control flow is depicted in Figure 14.

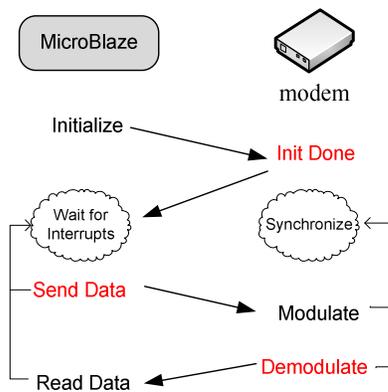


Figure 14. Modem Control Flow. Interrupts are shown in red

V. INITIAL RESULTS

In order to verify the operation of our modem, we first tested the analog components (the transducer and analog transceiver) and digital components (the digital transceiver) separately. For the analog testing, we took our modem hardware to Mission Bay, San Diego, CA and placed one transceiver and transducer on the dock to act as the transmitter and placed another transceiver and transducer on a boat to act as the receiver. The transmitter was powered by power supplies on the dock and the receiver was powered by a power supply connected to an inexpensive RadioShack AC/DC converter that unfortunately produced a substantial amount of noise (200mVpp).

We sent a 35kHz sinusoid from the transmitter to the receiver placed at three different locations as shown in Figure 15: 1. 75 meters, 2. 235 meters, and 3. 350 meter away. We were able to successfully detect the signal at 350m by applying 66Vrms across the transmit transducer, however the

receive signal was just above 200mVpp at this distance and hence could just be detected above the converter's noise.

This test proved that our analog hardware could transmit a considerable distance and would likely be able to transmit a much farther distance given a low-noise power supply at the receiver and further improvements to the analog transceiver.



Figure 15. Mission Bay Analog Transmitter and Receiver Locations

For digital testing, we purchased a prototype test platform, the DINI DMEG-AD/DA, that includes analog to digital and digital to analog converters, a Xilinx Virtex-4 FPGA, an onboard oscillator, and a serial port and downloaded the HW/SW co-design to the board. We set our initial test sequence as sending the 15 bit Gold Code of '011001010111101' followed by a 100 bit packet of randomized ones and zeros. We sent the signal through a 12 inch bucket of water and used the DINI board to synchronize and demodulate the data. Figure 16 shows a snapshot of the post place and route hardware simulation result for our digital modem design described in Verilog HDL.

The four signals in the figure are: the output signal of the down converter (*DDC out*), the output of the reference cross correlation block (*correlation*) used for synchronization, and the output of the two bandpass filters in the demodulator. In the *DDC out* signal one can observe the FSK realization of the Gold Code followed by the first 8 bits of data (the digital '0' being represented by the sparse waveform and the digital '1' being represented by the dense waveform). The bandpass filters are enabled in the demodulator when the correlation result first rises above the threshold (not shown). The vertical arrow labeled "Index" illustrates the synchronized peak found by the hardware which is a known clock delay from the start of the data (vertical arrow labeled "Actual"). The bit stream demodulated from the "Actual" peak are sent to the FSL buffer to be read by the MicroBlaze and printed to the Hyperterminal. The bits written to the Hyperterminal revealed 0% error rate for the 100 bit packet from the 12 inch plastic

bucket. The test was repeated with different data bits 10 times all producing 0% error.

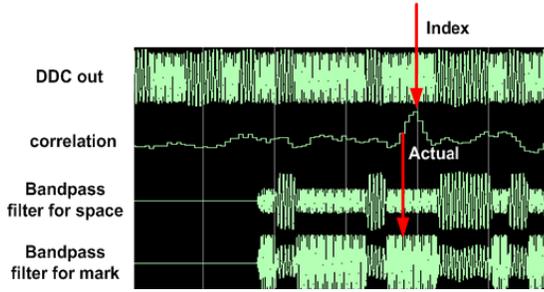


Figure 16. Snapshot of hardware simulation result for 12" bucket test

Because the bucket produced such perfect data, we generated data in Matlab with packet lengths of 10000 symbols and sent the signals to the hardware for synchronization and demodulation. These packets achieved a bit error rate of 10^{-2} at 10dB SNR.

Feeling confident that our analog and digital hardware components worked properly, we conducted an initial full system test at the UCSD Canyon View pool, a 50m x 25m concrete pool with 1m depth on the shallow end and 5m depth on the deep end. As the pool provided outdoor power outlets, we were able to power both the transmitter and receiver off power supplies.

At 50 meters distance, we sent a packet of 400 symbols followed by a 400 symbol clearing period followed by another packet of 400 symbols using only 6.5Vrms across the transmit transducer. The transducers were submerged to a depth of 10 cm and placed along the 50m side of the pool to avoid swimmers. The digital hardware was able to successfully detect the start of each packet, but failed to accurately demodulate the data, achieving 30% bit error rate. Figure 17 shows the first few symbols of the first received packet, at 10dB SNR, starting with the 15 symbol reference sequence followed by four data bits. The bold yellow vertical bar marks the start of the reference sequence (easily seen above the initial noise) and the light yellow vertical bar denotes what the synchronizer determined to be the start of data. *Sync_symbol_clk* denotes the symbol clock synchronized to the start of the first data symbol. *Adc_in* shows the input to the ADC, *ddc_out* shows the downconverted, downsampled signal used for all digital processing and *data_out* shows the demodulated bits.



Figure 17. Snapshot of 50m Canyon Pool Test Results

It can easily be seen in Figure 17 that the data can be accurately demodulated for the first few symbols of the received packet as there is a clear distinction between the mark and space frequencies. However, a strong multipath arrives at the receiver after about the 7th symbol, severely distorting the signal making accurate demodulation impossible. Concrete pools are one of the most difficult underwater channels due to extremely strong multipath and most other underwater acoustic modems fail in this environment.

Although we obtained 30% error rate in the concrete pool, we were encouraged by the results and are confident in an environment with less severe multipath, the modem can perform well. We are currently developing a power supply board, battery pack, and watertight housing (that can withstand pressures at depth of up to 100m) so we can test our modem in the open ocean in order to assess its true performance.

VI. MODEM COMPARISON AND CONCLUSION

Our anticipated cost and power estimates for the full modem prototype (not including batteries or housing) are shown in Table III. The power consumption of the analog transceiver depends on its mode. The interfaces (ADC and DAC) are specified as TBD (to be determined) as the ADC and DAC on our evaluation board are over specified and too power consuming for our intended design.

TABLE III.
COST AND POWER ESTIMATES FOR THE UNDERWATER MODEM

	Cost (\$)	Power (W)
Transducer	50	N/A
Transceiver	125	1- 40
Digital Components	75	0.2
Power Supply	100	TBD
Interfaces	TBD	TBD
Total	~\$250	

We compare our design with three commercial modems, two designed at private firms (LinkQuest and Teledyne Benthos) and one designed at Woods Hole Oceanographic Institute in Table IV. Note that the distance and bit rates reported for the modems are the maximum distance and rates achievable under ideal conditions. Also note that the price of the commercial modem designs is based on market prices whereas our design cost is based solely on parts costs and assembly labor. However the parts price of the commercial

TABLE IV. UNDERWATER ACOUSTIC MODEM COMPARISON

	Data rate	Transmission distance	Transmit & Receive power	Cost	Firmware and software design
Teledyne Benthos	2400 bps	2-6 km	12 W 0.4 W	\$10,000	Proprietary
LinkQuest	9600 bps	1500 m	4 W 0.8 W	\$8,000	Proprietary
WHOI Micro-Modem	80 bps (FH-FSK) 300-5400 (PSK)	1-10 km	10-100 W 200 mW – 2W	\$8,000	All design information is available online.
UCSD Modem	200 bps	2 km	1 – 40 W 1W	\$600	All design information will be available online.

modems is still much more than the full price of our modem as commercial transducers used in the designs solely cost a few thousand dollars.

From this comparison we observe that our modem currently stands as low-cost, comparable power alternative to existing modem designs. In the future, to further reduce power consumption, we plan to explore the possibilities to provide signal detection at even lower power levels. This is paramount to building a modem that has low listening power, which is also a key requirement to ensure long lifetime on a limited battery supply. We plan to eventually utilize a design that has a programmable gain, which is dynamically controlled by the digital hardware platform. In addition, further changes to the circuit design of the transceiver will be made to further increase its efficiency and digital transceiver implementations of advanced modulation techniques will be explored.

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